Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE YIELD

Inventor: Eitan CADOURI
Application No.: Not Yet Assigned

Sheet 1 of 6

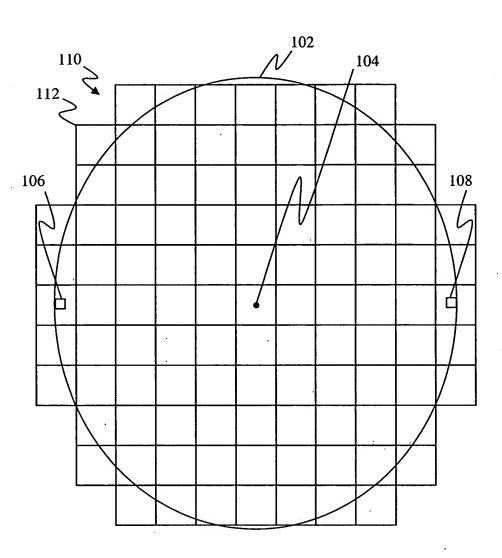


Fig. 1

Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE YIELD Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 2 of 6

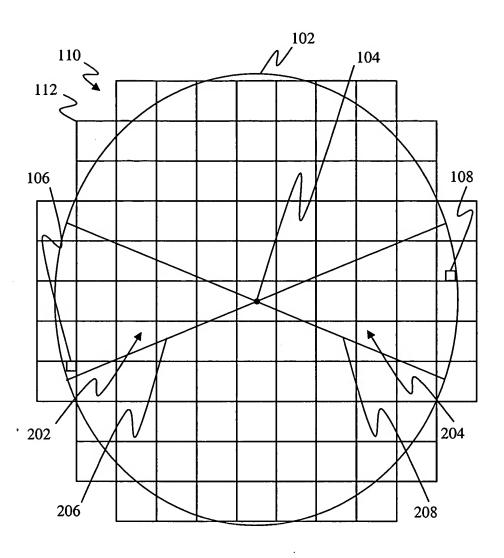


Fig. 2

Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE

YIELD

Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 3 of 6

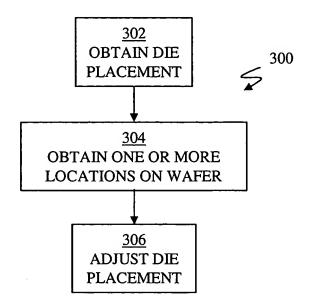


Fig. 3

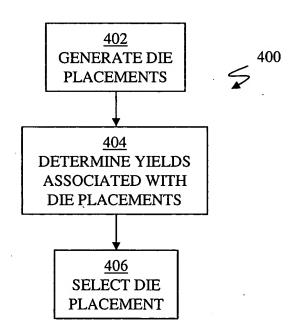


Fig. 4

Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE YIELD

Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 4 of 6

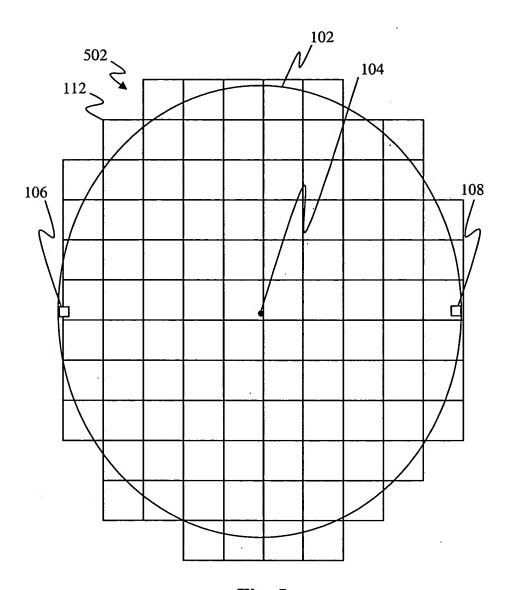


Fig. 5

Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE

YIELD

Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 5 of 6

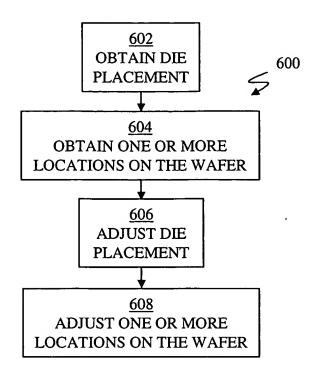


Fig. 6

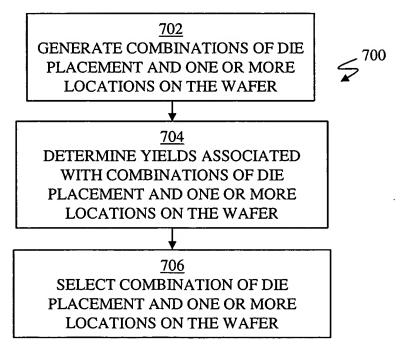


Fig. 7

Title: ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE YIELD Inventor: Eitan CADOURI Application No.: Not Yet Assigned

Sheet 6 of 6

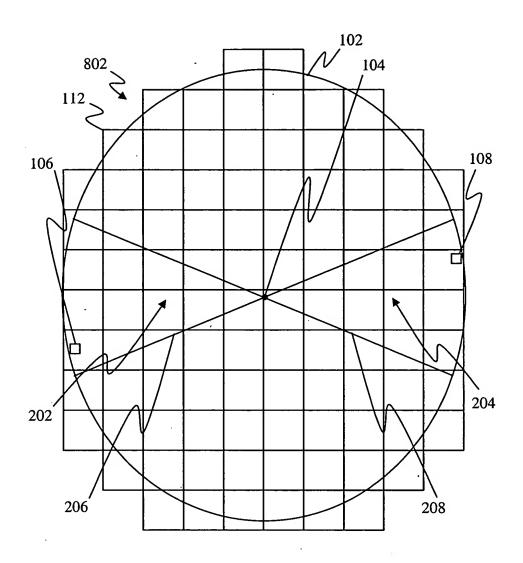


Fig. 8